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PRE-APPEAL BRIEF REQUEST FOR REVIEW		Docket Number (Optional) LSI.83US01 (03-1818)	
I hereby certify that this correspondence is being facsimile transmitted to the USPTO (571-273-8300) under 37 CFR §1.8		In re Application of Matthew Trembley	
on <u>February 10, 2006</u>		Application Number 10/687,991	
Signature <u>Kathy M. Manke</u>		Filed October 17, 2003	
Typed or printed name <u>Kathy M. Manke</u>		For METHOD FOR DETECTING MEMORY PAGE BOUNDARIES WITH A PROGRAMMABLE PAGE SIZE	
		Art Unit 2819	
		Examiner Don P. Le	
<p>Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.</p> <p>This request is being filed with a notice of appeal.</p> <p>The review is requested for the reasons stated on the attached sheets.</p> <p>I am the</p> <div style="display: flex; justify-content: space-between;"> <div style="width: 45%;"> <p><input type="checkbox"/> applicant/inventor.</p> <p><input type="checkbox"/> assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)</p> <p><input checked="" type="checkbox"/> attorney or agent of record. Registration number <u>26,652</u></p> <p><input type="checkbox"/> attorney or agent acting under 37 CFR 1.34. Registration number if acting under 37 CFR 1.34. _____</p> </div> <div style="width: 45%; text-align: center;">  <hr/> <p>Signature</p> <hr/> <p>William W. Cochran</p> <hr/> <p>Typed or printed name</p> <hr/> <p>970-492-1100</p> <hr/> <p>Telephone number</p> <hr/> <p>February 10, 2006</p> <hr/> <p>Date</p> </div> </div> <p>NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below.</p>			
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventors: Kevin T. Campbell et al.

Examiner: Don P. Le

Serial No.: 10/687,991

Group Art Unit: 2819

Filed: 10/17/2003

Docket: LSI.83US01 (03-1818)

Title: METHOD FOR DETECTING MEMORY PAGE BOUNDARIES WITH A
PROGRAMMABLE PAGE SIZE

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PRE-APPEAL BRIEF REQUEST FOR REVIEW

Dear Sir:

Applicants hereby submit a Pre-Appeal Brief Request for Review in accordance with the Pre-Appeal Brief Conference Pilot Program. Applicants make the following statement:

Claims 1, 4, 5, 8, 10, 14, 16 and 17 were rejected under 35 USC § 102(b) as being anticipated by Mori.

Mori discloses a system for determining the existence of a selected size and orientation of copy papers for use in a copying machine. The Mori system is useful for copying using various magnification ratios. Mori discloses orientation indicators and size indicators for the selected copy paper so that when installed copy papers do not satisfy the condition required by a desired mode of copying operation, it will be clearly indicated whether the size and/or the orientation of the installed copy papers are appropriate.

The Mori disclosure differs substantially from Applicant's claimed invention. For example, claim 1 recites "a method for detecting a page boundary in data stream." The term page boundary in this context refers to the manner in which a data stream is divided into groups of data called pages. Pages, in this case, do not refer to paper, as disclosed in

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Mori. The preamble of claim 1 specifically recites that the page boundary relates to “a data stream.” One skilled in the art would certainly recognize that the “page boundary” referred to in the preamble of claim 1 refers to the division of a data stream into pages or groups of data, and not to paper copies.

Furthermore, the term “page boundary” and “page size” are specifically defined in the specification. For example, on page 3, lines 8-21, the application specifically recites:

Figure 1 illustrates an embodiment 100 of the present invention showing a logic circuit for the detection of page boundaries. A binary address input 102 and a predetermined page size 104 are input to a logic operator 106. The output of the logic operator and a predetermined value 110 are input into a bit-by-bit comparator 108 to generate an output signal 112.

The embodiment 100 may be used to monitor a data stream and to cause some action to occur at regular intervals in the data stream. For example, in a large data stream, it may be useful to compute a cyclic redundant check or CRC for specific intervals in the data. The CRC may be stored with the data and used to verify data integrity in subsequent operation. At a regular interval determined by the pre-determined page size 104, the embodiment 100 will cause the output signal 112 to change state. The output signal 112 may trigger a CRC to be calculated or other function to occur. Those skilled in the arts will appreciate that various functions may be triggered by the output signal 112. (Emphasis Added)

These two paragraphs in the specification clearly define that a “page boundary” and “page size” are created at regular intervals in a data stream. This has nothing to do with paper copies. Applicants have a right to be their own lexicographer and define terms that are used in the claims. In this case, Applicants have clearly defined the term “page boundary” and “page size” which relate to the grouping of data in a data stream and not paper copies. Both the claims and specification provide these definitions. Hence, the Mori disclosure is irrelevant to that which is claimed in claim 1.

Further, claim 1 recites “determining a page size.” This step is also recognized by those skilled in the art and defined in the specification as determining the amount of data that is to be included in a group or page in which the data stream is divided. There is no disclosure in Mori of such a step. Rather, the Examiner points to the step in Mori of determining size of a piece of paper. Mori determines the size and orientation of copy paper to make sure that the proper copy paper is selected that will fit the image to be

copied. It is clear, that the step of "determining a page size" to those skilled in the art is not selecting the size of a piece of paper, but selecting a page size in a data stream.

Similarly, the step of storing the page size is not performed by Mori. Also, the step of receiving a data stream address is not disclosed in Mori. The Examiner argues that the encoder A1 performs this function, but there is no disclosure of a data stream and an associated address, as set forth in claim 1. Similarly, the step of performing a Boolean logic operation on the data stream address and the page size, comparing the binary output and causing the boundary signal to change state are also not performed by Mori. For these reasons, the rejection of claim 1 as being anticipated by Mori should be withdrawn.

Claim 10 has similar limitations as claim 1 and is considered to be patentable for the same reasons. Claims 4, 5, 8, 14, 16 and 17 are all considered to be patentable for the same reasons as recited with respect to claim 1.

In addition, claims 19 and 20 are considered to be allowable for the same reasons as claims 1 and 10, as set forth above. Claims 19 and 20 further define the manner in which a page size is selected and the manner in which the address of the data stream relates to the data in the data stream.

Claims 2, 3, 5-7 and 11-13 were rejected under 35 USC § 103(a) as being unpatentable over Mori in view of Mano. The Examiner argued that Mano discloses an XOR, with equivalent circuits having other logic operators such as AND, NAND, OR and NOR. The Examiner argues that it would be obvious to implement the various other logic gates such as AND, NAND, OR and NOR in view of the teachings of Mano.

Mano does not make up for the deficiencies of Mori. There is no disclosure in Mano or Mori of "a method of detecting a page boundary in a data stream" as defined in the specification and as would be understood by one of ordinary skill in the art. Further, it appears unlikely that a substitution of other logic gates in Mano would allow Mano to operate as intended. For the reasons set forth above, claims 2, 3, 5-7 and 11-13 are considered to be patentable over the combination of Mori and Mano.

Claims 9 and 18 were rejected under 35 USC § 103(a) as being unpatentable over Mori. The Examiner argued that Mori does not specifically disclose the circuit as part of an integrated circuit and that it is well known in the art that logic gates and memories can be implemented on an integrated circuit.


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Claims 9 and 18 are considered to be allowable for all the same reasons as claims 1 and 10.

For these reasons, this application is considered to be in condition for allowance and such action is earnestly solicited.

Dated this 10th of February, 2006.

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